WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a plurality of fin structures comprising a crystalline silicon material;

a source region formed at one end of the fin structures;

a drain region formed at an opposite end of the fin structures; and

at least one gate.

2. The semiconductor device of claim 1, wherein a width of each of the fin structures ranges from about 100 Å to about 1000 Å.

3. The semiconductor device of claim 1, wherein the plurality of fin structures is two fin structures.

4. The semiconductor device of claim 1, wherein a pitch associated with the fin structures is about 600 Å.

5. The semiconductor device of claim 1, wherein a height of each of the fin structures ranges from about 500 Å to about 2000 Å.

6. A method of forming fin structures for a semiconductor device that includes a substrate and a dielectric layer formed on the substrate, the method comprising:

etching the dielectric layer to form a first structure;

depositing an amorphous silicon layer over the first structure;

etching the amorphous silicon layer to form second and third fin structures adjacent first

and second side surfaces of the first structure, the second and third fin structures including amorphous silicon material;

depositing a metal layer on upper surfaces of the second and third fin structures;

performing a metal-induced crystallization operation to convert the amorphous silicon material of the second and third fin structures to a crystalline silicon material; and

removing the first structure.

7. The method of claim 6, wherein a width of the first structure ranges from about 200 Å to about 1000 Å.

8. The method of claim 6, wherein the dielectric layer comprises at least one of an oxide and a nitride.

9. The method of claim 6, wherein a width of each of the second and third fin structures ranges from about 100 Å to about 1000 Å.

10. The method of claim 6, wherein the etching the dielectric layer includes:

thinning the first structure using an additional etching process.

11. The method of claim 6, wherein the depositing a metal layer includes:

depositing a nickel layer to a thickness of about 20 Å.

12. The method of claim 6, wherein the etching the amorphous silicon layer includes:

etching the amorphous silicon layer to form a plurality of fin structures, wherein the plurality of fin structures includes more than two fin structures.

13. The method of claim 6, wherein the performing a metal-induced crystallization operation includes:

annealing the semiconductor device at a temperature of about 500 °C to about 550 °C.

14. The method of claim 13, wherein the annealing is performed for at least two hours.

15. A semiconductor device, comprising:

a substrate;

a plurality of crystalline silicon fin structures formed on the substrate, a center-to-center distance between each of the fin structures being about 600 Å;

a source region formed at one end of the fin structures;

a drain region formed at an opposite end of the fin structures; and

one or more gates.

16. The semiconductor device of claim 15, wherein a width of each of the fin structures ranges from about 100 Å to about 1000 Å.

17. The semiconductor device of claim 15, wherein the plurality of fin structures is two fin structures.

18. The semiconductor device of claim 15, wherein the plurality of fin structures is more than two fin structures.

19. The semiconductor device of claim 15, wherein a height of each of the fin structures ranges from about 500 Å to about 2000 Å.